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IN RE APPLICATION OF:	:
YOUNG-HUN SEO	: GROUP ART UNIT: 2813
APPLICATION NO: 10/722,295	:
FILED: AUGUST 25, 2003	: EXAMINER: CHEN, JACK S J

FOR: METHOD OF FORMING TRENCH IN SEMICONDUCTOR DEVICE

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By: Jennie Heaton
Jennie Heaton

DECLARATION UNDER 37 C.F.R. 1.132

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SIR:

Now comes Young-Hun SEO, who declares and states that:

1. I am currently employed by Dongbu Electronics Co., Ltd., the assignee of the entire interest of the above-identified application, as a Director. My responsibilities include managing and performing research, development and production activities relating to etch processes at the Bucheon Fab of Dongbu Electronics Co., Ltd. I have been continuously employed by Dongbu Electronics Co., Ltd. since Feb. 22, 1998.

2. I received a Bachelor's degree in Chemical Engineering from Chungbuk National University in Chonju, Korea.

3. I have read and am familiar with the subject matter disclosed and claimed in the above-identified application. I have also read U.S. Patent Nos. 6,884,725 (to Moore et al.) and 6,890,859 (to Bamnolker et al.), and I am knowledgeable about the subject matter disclosed therein.

4. I understand that claim 1 of the above-identified application is directed to a method of forming a trench in a semiconductor device comprising:

(a) forming a polish stop layer on a semiconductor substrate;

(b) forming an organic anti-reflection coating on the polish stop layer;

(c) selectively etching the anti-reflection coating to form an anti-reflection coating pattern;

(d) etching the polish stop layer and the semiconductor substrate such that ends of the polish stop layer are rounded along substantially the entire thickness of the polish stop layer, and a trench having sloped sidewalls is formed to a predetermined depth; and

(e) forming an insulation layer that fills the trench.

5. The method defined in paragraph 4 above provides improved results (e.g., a trench-fill capability) that are not disclosed, suggested or appreciated by the patents to Moore et al. and Bamnolker et al.

6. Etching the polish stop layer such that ends of the polish stop layer are rounded along substantially the entire thickness of the polish stop layer enables filling a relatively narrow trench in the substrate with an insulation layer using previous-generation trench-filling equipment in commercially acceptable yields.

7. Shallow trench isolation (STI) is frequently used to form isolation structures in a semiconductor device. In STI, a trench is formed in a semiconductor substrate, and an insulation material is filled in the trench. It is important in STI to completely fill the trench with the insulation material, without the formation of voids, which can lead to defects in the devices and reduced yields. (Also see paragraphs [0002]-[0003] of the specification.)

8. In semiconductor manufacturing processes having a critical dimension of 0.18 μm or less, one typically needs trench-filling equipment designed for filling trenches having a width at or near the critical dimension. The term "critical dimension" refers to a minimum design rule, or the minimum width for a structure or feature on the semiconductor device that can be reliably made using a given set of photolithography and other processing equipment.

9. Such trench-filling equipment adds considerable cost to the semiconductor manufacturing process, and consumes valuable floor space in a wafer fabrication facility ("fab") that is configured for manufacturing wafers using processes having a critical dimension of 0.18 μm or less, as well as manufacturing processes having a critical dimension of more than 0.18 μm (e.g., 0.25 μm).

10. The benefit of using the same trench-filling equipment for both types of manufacturing processes (i.e., having a critical dimension of 0.18 μm or less, and having a critical dimension of, e.g., 0.25 μm) is commercially significant, in terms of reducing the cost of wafers manufactured on processes having a critical dimension of 0.18 μm or less, maximizing the investment in trench-filling equipment for manufacturing processes having a critical dimension of more than 0.18 μm (e.g., 0.25 μm), and maximizing efficiency of floor space in a fab configured for manufacturing wafers using both types of manufacturing processes.

11. Based on my knowledge of actual production data for manufacturing processes having a critical dimension of 0.18 μm or less, etching the polish stop layer such that ends of the polish stop layer are rounded along substantially the entire thickness of the polish stop layer enables filling a trench in the substrate with an insulation layer using trench-filling equipment designed for manufacturing processes having a critical dimension of more than 0.18 μm (e.g., 0.25 μm) in commercially acceptable yields.

12. Based on my knowledge of data generated during development of a manufacturing process having a critical dimension of 0.18 μm, etching the polish stop layer such that ends of the polish stop layer are not significantly rounded results in an unacceptably high incidence of void formation when filling a trench in the substrate with an insulation layer using trench-filling equipment designed for manufacturing processes having a critical

dimension of more than 0.18 μm (e.g., 0.25 μm). The defect rates in semiconductor devices manufactured using such etching and trench-filling steps are commercially unacceptable, and lead to commercially unacceptable yields.

13. This difference in trench-filling capability between the method defined in paragraph 4 above and an otherwise comparable process in which ends of the polish stop layer are not significantly rounded is unexpected; in other words, prior to my invention, one of ordinary skill in the art(s) of semiconductor processing and/or manufacturing would not have predicted that etching the polish stop layer such that ends of the polish stop layer are rounded along substantially the entire thickness of the polish stop layer would enable filling a trench in the substrate using a manufacturing process having a critical dimension of 0.18 μm with an insulation layer using trench-filling equipment designed for manufacturing processes having a critical dimension of more than 0.18 μm (e.g., 0.25 μm) in commercially acceptable yields.

14. I also understand that claims 2-4, 8-10 and 15-17 of the above-identified application further limit the method of claim 1, wherein etching the polish stop layer comprises injecting one or more of CHF_3, CF_4, O_2, HeO_2, and Ar, creating a plasma and dry etching the polish stop layer.

15. The present application discloses the subject matter described in paragraph 6 above. Thus, one skilled in the art of semiconductor processing and/or manufacturing understands that the subject matter described in paragraph 14 above (e.g., "injecting one or more of CHF_3, CF_4, O_2, HeO_2, and Ar") is supported by the application as originally filed.

16. For example, the present specification discloses:

(a) "Dry etching" the silicon nitride (polish stop) film 13, the pad oxidation layer 12 and the semiconductor substrate 11 form a trench 100 (see paragraph [0030], p. 7 of the application as originally filed); and

(b) Forming "a sidewall polymer" during dry etching (see paragraph [0033], p. 8 of the application as originally filed).

17. One skilled in the art of semiconductor processing and/or manufacturing understands that the disclosures cited in paragraph 16 above encompasses mixtures of the etchants recited in paragraph 14 above. As a result, claims 2-4, 8-10, and 15-17 of the present application are supported by the specification as originally filed.

18. For example, one skilled in the art understands that forming a sidewall polymer occurs when dry etching SiO_2 (e.g., a material suitable for pad oxidation layer 12) and silicon nitride (SiN; a material suitable for polish stop layer 13) with a fluorocarbon plasma (see, e.g., Wolf, "Silicon Processing for the VLSI Era," vol. 1, pp. 672-673 and 678-683, particularly p. 672, Table 14-2; p. 678, Fig. 14-17 and the first paragraph therebelow; p. 680, Fig. 14-19(b) and paragraph #2; and p. 683, lines 3-4, the first full paragraph, and Fig. 14-23; attached hereto as part of Exhibit A). Notably, Wolf teaches the well-known formation of sidewall polymer in a process that etches a trench into silicon under a layer of SiO_2 (a well-known structure resulting from the oxidation of silicon) using a mixture of CHF_3 and CF_4 (both of which are recited in paragraph 14 above), or a mixture of a fluorocarbon and O_2 (also recited in paragraph 14 above; see also Wolf, p. 683, the first paragraph, ll. 11-16, and Fig. 14-23).

19. It is known in the art that a very similar sidewall polymer is formed when etching silicon nitride (a well-known mask layer for etching a trench into a silicon substrate) with fluorocarbon-based etchant. Therefore, one skilled in the art(s) of semiconductor devices and semiconductor manufacturing would readily understand that the present specification inherently discloses and supports dry etching a silicon nitride (polish stop) layer and a semiconductor substrate using a mixture of the etchants recited in paragraph 14 above, notably a mixture of the CHF_3, CF_4 and/or O_2 etchants.

20. O_2 itself does not dry etch silicon nitride, SiO_2 or Si (see also, e.g., Wolf, p. 672, Table 14-2). As a result, one skilled in the art would understand that, to the extent O_2 is used in the etching step as recited in paragraph 14 above, the silicon nitride (polish stop) film 13, the pad oxidation layer 12 and the semiconductor substrate 11 must be etched with a mixture of O_2 and another etchant (e.g., CF_4; also see Wolf, p. 673, first paragraph of section 14.4, and Table 14-2 on p. 672). Any disclosure to the effect that silicon nitride, SiO_2 or Si is dry etched with O_2 alone is an error that is readily apparent to those skilled in the art.

21. As a result, one skilled in the art(s) of semiconductor devices and semiconductor manufacturing would further understand that the present specification application as originally filed discloses dry etching a silicon nitride (polish stop) layer 13 and a pad oxidation layer 12 to form a trench in a semiconductor substrate using a mixture of the etchants including CF_4, CHF_3, and/or O_2 as recited in paragraph 14 above.

22. In addition, the present specification discloses that the antireflection coating ARC 14 may be a conventional ARC made of an organic material (p. 7, l. 7-8 of the specification), and that dry etching to form the trench 100 can be controlled such that a small amount of exposed ends of the ARC layer 14 is removed (p. 7, l. 20-p. 8, l. 1 of the specification).

23. As is known in the art, dry etching an organic solid (such as the embodiment of the ARC 14 disclosed by the present specification and discussed in this paragraph) can be done with O_2 alone or in combination with CF_4 (see Wolf, p. 672, Table 14-2). As a result, one skilled in the art(s) of semiconductor devices and semiconductor manufacturing would understand that the present application as originally filed discloses dry etching an organic ARC using one or more of the etchants recited in paragraph 14 above, including a mixture of the O_2 and CF_4 etchants.

24. One skilled in the art also understands that *molecular* gases are used in dry etching (see, e.g., Wolf, pp. 668-9, particularly p. 669, l. 7, attached hereto as part of Exhibit A; emphasis in original). One of the gases recited in paragraph 14 above, Ar (argon), is not a molecular gas. Accordingly, one skilled in the art understands that Ar is not used alone in dry etching (see also, e.g., Wolf, p. 679, the second full paragraph, which teaches the well-known use of Ar ions to *assist* dry etching processes). One skilled in the art therefore understands from the application as originally filed that dry etching uses a molecular gas such as CHF_3, CF_4, O_2, or HeO_2, and the disclosure of Ar as a gas for use in dry etching must refer to its use in combination with one (and possibly more) of the molecular gases recited in paragraph 14 above. Any disclosure to the effect that silicon nitride, SiO_2 or Si is dry etched with Ar alone is an error that is readily apparent to those skilled in the art.

25. Thus, the present application as originally filed discloses etching a polish stop layer and a pad oxidation layer to form a trench in a semiconductor substrate using a mixture of Ar and at least one of the CHF_3, CF_4, O_2, and HeO_2 etchants recited in paragraph 14 above.

Further, Declarant sayeth not.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the above-identified application or any patent issued thereon or therefrom.

Sto. Young-Hun — 2006. 10. 30.

Signature — Date

Young-Hun SEO

Name

EXHIBIT A

SILICON PROCESSING

FOR

THE VLSI ERA

VOLUME 1:

PROCESS TECHNOLOGY

Second Edition

STANLEY WOLF Ph.D.

RICHARD N. TAUBER Ph.D.

LATTICE PRESS

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surface; and 6) the desorbed species diffuse into the bulk of the gas, and are pumped from the chamber (#7 in Fig. 14-10).[11] If any of these steps fails to occur, the overall etch cycle ceases. Step 5 (product desorption) is a noteworthy step. Many reactive species can react rapidly with a solid surface, but unless the product has a reasonable vapor pressure so that desorption occurs, no etching takes place. Also note that steps 1, 2, and 6 involve events occurring in the gas phase and plasma, while steps 3, 4, and 5 take place at the surface of the solid layer being etched. Hence, it is useful to briefly consider the physics and chemistry of events that involve the etching process that occur in: a) the plasma; and b) the surface being etched.

Finally, as seen in Fig. 14-10 other significant effects can also be occurring, including: 1) ion bombardment (of the wafer surface and the chamber walls), which can assist in etch-product desorption from the wafers and erosion of materials from the chamber walls; and 2) deposition (or re-deposition) of some of the gas-phase molecular fragments and etching products on the wafer surfaces and chamber walls.

14.3.1 The Reactive-Gas Glow Discharge

In Chap. 11 the methods for producing a glow-discharge using a dc diode and an rf diode configuration are described. In conventional plasma-etching processes (i.e., not a high-density plasma process) an rf diode configuration is used to establish the glow discharge (for the reasons listed in Chap. 11). The glow discharge in Chap. 11 was treated primarily as a phenomenon that

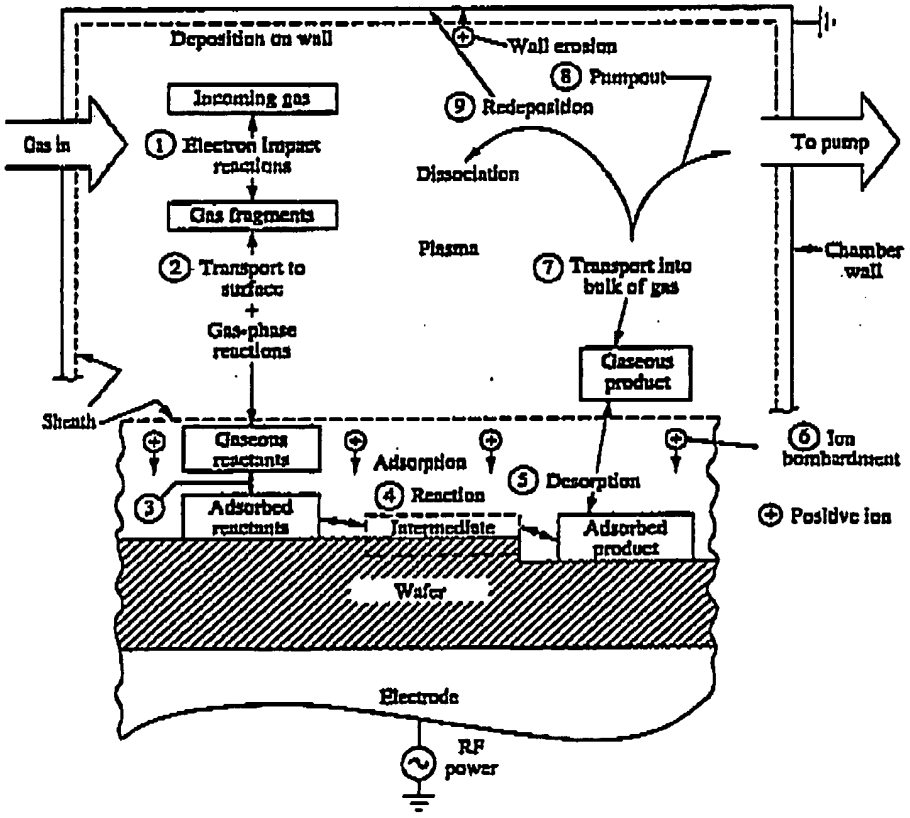

Fig. 14-10 Schematic view of the microscopic processes that occur during the etching of a silicon wafer.[11]

produces energetic ions, which are then in turn used to bombard target surfaces and cause sputtering. As such, the plasma gases used in sputtering are *atomic*, non-chemically reactive gases (such as Ar). In plasma etching applications the glow discharge is not only used to produce energetic ionic bombardment of the etched surface, but it has another even more important role, namely that of producing reactive species for chemically etching the surfaces of interest. Thus, it is necessary to examine the properties of glow discharges related to this function. Note that that *molecular* gases are used in dry etching. Gases selected are either inherently reactive (such as Cl_2), or can be dissociated into molecular fragments (that are then reactive - for example, CF_4, a molecule that can be dissociated into such reactive species as F, CF_3, CF_3^+, etc.).

Since plasmas consisting of fluorine-containing gases are extensively used for etching Si, SiO_2, Si_3N_4, and other materials used in ULSI fabrication, it is appropriate to study the glow discharge created in a CF_4 gas as an example. Before a glow discharge is established in such a gas, the only species present are CF_4 molecules. Over the pressure range at which an rf glow discharge can be maintained: 1 Pa–750 Pa (or 7.5 mtorr–5.6 torr), the gas density ranges from 2.7×10^{14}–2×10^{17} molecules/cm^3. When the glow-discharge has been formed, some fraction of the CF_4 molecules are dissociated into other species.

A plasma is defined to be a partially ionized gas composed of ions, electrons, and a variety of neutral species. A glow discharge is a plasma that exists in the pressure range given above and contains approximately equal concentrations of positive particles (positive ions) and negative particles (electrons and negative ions). The density of these charged particles in conventional (i.e., low density plasma) glow discharges ranges from 10^9–10^{11}/cm^3. Thus, only one atom in 10^4–10^6 of the gas is ionized in a low-density glow discharge. The average energy of electrons in glow discharges is between 1–10 eV. The reactions that occur in the gas phase (plasma) are called *homogeneous* reactions, while those that occur at the surface are termed *heterogeneous* reactions. Table 14-1 lists the general types of homogeneous electron-impact reactions and heterogeneous surface-plasma reactions that can take place.

Table 14-1 HOMOGENEOUS REACTIONS (CAUSED BY ELECTRON-IMPACT) AND HETEROGENEOUS REACTIONS THAT OCCUR IN PLASMAS

Homogeneous Reactions - (Electron Impact Reactions)	Heterogeneous Reactions
Excitation (rotational, vibrational, electronic):	S = Surface
$e + A_2 \Rightarrow A_2 + e$ $(e + F \rightarrow F^* + e)$	Atom Recombination at a Surface:
$(F^* \rightarrow F + h\nu_F)$	$S + A + A \Rightarrow S + A_2$
	Metastable de-excitation:
Dissociation:	$S + M^* \Rightarrow S + M$
$e + A_2 \Rightarrow A + A + e$ $(e + O_2 \Rightarrow O + O + e)$	Atom abstraction (etching):
Ionization:	$S + B + A \Rightarrow S^+ + AB$
$e + A_2 \rightarrow A_2^+ + 2e$ $(e + O_2 \rightarrow O_2^+ + 2e)$	Sputtering (etching):
Dissociative Ionization:	$S\text{-}B + M^+ \Rightarrow S^+ + B + M$
$e + A_2 \rightarrow A^+ + A + 2e$ $(e + O_2 \Rightarrow O^+ + O + 2e)$	
Dissociative Attachment:	
$e + A_2 \rightarrow A^+ + A^- + e$	

Table 14-2 EXAMPLES OF SOLID-GAS SYSTEMS USED IN PLASMA ETCHING

SOLID	ETCH GAS	ETCH PRODUCT
Si, SiO_2, Si_3N_4	CF_4, SF_6, NF_3	SiF_4
Si	Cl_2, CCl_2F_2	$SiCl_2$, $SiCl_4$
Al	BCl_3, CCl_4, $SiCl_4$, Cl_2	$AlCl_3$, Al_2Cl_6
Organic Solids	O_2	CO, CO_2, H_2O
	O_2 + CF_4	CO, CO_2, HF
Refractory Metals (W, Ta, Mo...)	CF_4	WF_6, --

ions depends upon whether they strike the bottom, or the sidewall of an etched feature).

The gases adopted for plasma etching processes have been selected on the basis of their ability to form reactive species in a plasma, which then react with the surface materials being etched and lead to volatile products. Table 14-2 lists the solid-gas systems for various solids to be etched in ULSI fabrication, together with their resultant etch products.

14.3.4 Parameter Control in Plasma Processes

One of the more challenging aspects of implementing a useful and reproducible etch process involves the control of the large number of parameters that affect the process. Figure 14-12 illustrates some of the parameters that impact the gas-phase interactions, as well as the surface-plasma interactions. Many macroscopic parameters can be controlled, such as the type of feed

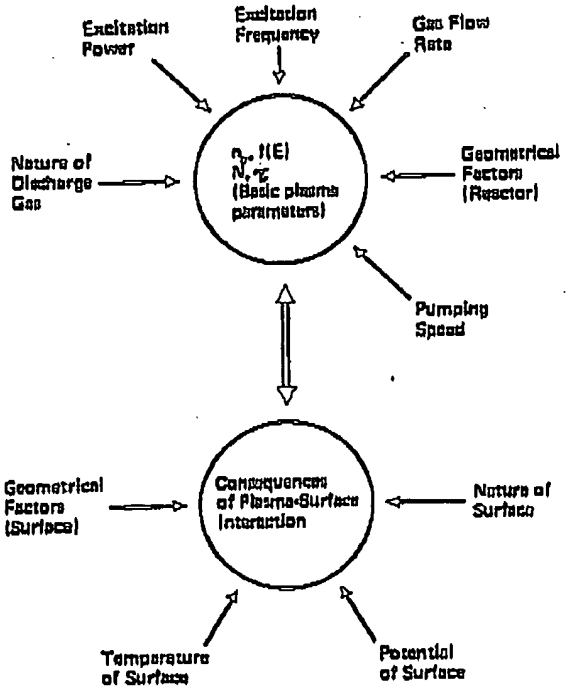

Fig. 14-12 Representation of the parameter problem in plasma etching systems (n_e is the electron density, f(E) is the electron energy distribution function, N is the gas density, and τ is the residence time.[15] Reprinted with permission of Springer-Verlag Publishing Company.

gas, power, and pressure. However, the precise effect of making any changes in these parameters is usually not well understood. In fact, a change in a single macroscopic parameter typically alters two or more basic *plasma* parameters, and possibly one or more of the surface parameters (such as temperature or electrical potential). This makes process development in plasma systems a challenge, and the use of factorial experimental design techniques for such tasks very useful.[16] In the introduction to the Sect. 14.8 on *Dry-Etch System Configurations*, a discussion is presented on how gas flow, pumping speed, and pressure are interrelated, and how this interrelationship is used to control pressure.

14.4 ETCHING SILICON AND SILICON DIOXIDE IN FLUOROCARBON PLASMAS

The etching of silicon and SiO_2 in fluorocarbon plasmas is described here in substantial detail. This is because these etching processes are very important in silicon ULSI fabrication. When the mechanisms of plasma etching were being first studied, the etching of silicon and SiO_2 in plasmas containing CF_4, mixtures of $CF_4 + O_2$, and mixtures of $CF_4 + H_2$ yielded important data about many of the fundamental mechanisms that are operative in plasma etching, as well as information about the specific materials system under investigation. The conclusions from these studies led to the development of two models for organizing chemical and physical information on plasma etching. These models are the *fluorine-to-carbon ratio model (or F/C model)*,[17] and the *etchant-unsaturate model*.[18] Since the models are conceptually similar (although they emphasize different aspects of plasma etching), only the F/C model will be described. For details of the etchant-unsaturate model, see Ref. 19.

Several basic phenomena related to plasma etching processes are considered first. It is known that in the absence of a glow discharge the gases commonly used in plasma etching do not react with the surfaces to be etched. For example, CF_4 does not etch silicon or silicon dioxide without a discharge. This is due to the fact that CF_4 does not chemisorb on Si and SiO_2 surfaces, and thus Step 3 of the dry-etching process described earlier does not occur. On the other hand, molecular fluorine has been found to spontaneously etch Si, even without the presence of a discharge (Fig. 14-13).[20] (Note that although F_2 itself etches silicon, it leaves a rough and pitted surface, and is thus not used as feedstock gas in IC etching processes of silicon.) Thus, when a discharge of CF_4 is created, it is not the CF_4 molecules themselves that participate

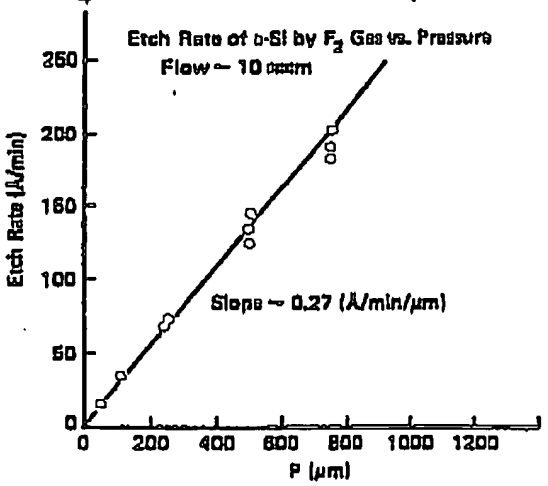

Fig. 14-13 The fluorine pressure dependence of the etch rate of amorphous silicon at room temperature.[20] Reprinted with permission of the publisher, the Electrochemical Society.

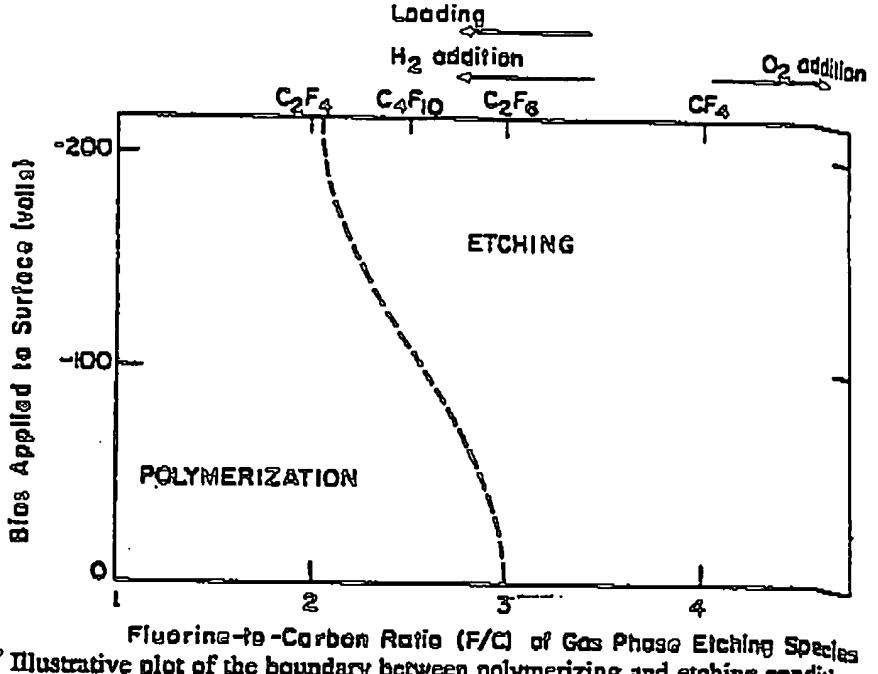

Fig. 14-17 Illustrative plot of the boundary between polymerizing and etching conditions as influenced by the fluorine-to-carbon ratio of the chemically reactive species and the bias applied to a surface in the discharge.[17] Reprinted with permission of the American Physical Society.

14.5 ANISOTROPIC ETCHING AND CONTROL OF EDGE PROFILE

Up to this point the etching of Si and SiO_2 in fluorocarbon plasmas largely as a mechanism that proceeds by chemical action (i.e., the reaction of Si by F-atoms generated by the plasma to form SiF_4) has been discussed. If etching action is purely chemical, however, the removal of material is isotropic, and no advantage in dimensional control is gained over wet etching. In such processes, the plasma plays no role other than to produce the etchant. The potential attraction of dry-etching for ULSI patterning, however, is based on the possibility that it can etch in an anisotropic manner. Thus mechanisms that could produce anisotropic etching need to be considered.

The desired degree of directionality varies with the specific application in the final device. For example if the lines etched from a deposited film are designed to carry current, steep-walled profiles are preferred, so that the cross-sectional area of the conductor is maximized for a fixed amount of chip area.

If an etched feature must be subsequently covered by another film, tapered profiles on the walls of the etched feature may be more desirable, since highly anisotropic profiles in underlying topography may result in poor step coverage by the overlying film. As mentioned earlier, a highly anisotropic etch will cause "stringers" in the overlying film to be left behind at the base of steep underlying steps (Fig. 14-6). Since such stringers represent regions of incomplete etching between adjacent lines, the etch process must remove them. This can be done in several ways including: a) overetching the overlying film; b) introducing a finite lateral etching component into the etch process; and c) insuring the underlying feature steps have tapered wall profiles. Achieving wall profiles with the desired degree of slope may require the use of a multi-step etch process, in which each of the sub-processes would employ of an etch mechanism with its own degree of anisotropy. A multi-step etch process for producing arbitrarily shaped wall profiles by such piece-wise anisotropic etching is described in Ref. 25.

The ability to achieve anisotropic etching is thought to depend in some way on the bombardment of the etched surface with energetic ions. Other parameters, such as the chemical nature of the plasma, may influence the degree of anisotropy, but unless energetic particles strike a surface, only isotropic etching can be expected. The directional etching effects in ion-assisted etching processes, however, cannot be due to sputtering alone, as product yields of over several hundred substrate atoms per incident ion have been reported in ion-assisted etch processes. Such product yields are much greater than those of typical sputtering yields (e.g., < 2 for 400 eV Ar ions, see Chap. 11). This is fortunate, for as was discussed earlier, purely sputter etch mechanisms result in processes with inadequate selectivities.

The fact that sputtering alone is not operative in such processes, was elegantly demonstrated in an experimental manner by Coburn and Winters.[26] They first exposed a Si surface to a gas of XeF_2 (not a plasma of XeF_2), and observed a low etch rate.(Fig. 14-18). Next, while continuing to expose the surface to XeF_2, an Ar^+ ion beam with an energy of 450 eV was directed at the Si. The observed etch rate was ~10 times as great as with the XeF_2 alone. Finally, when the Ar^+ beam alone was directed at the surface, the smallest etch rate of the three conditions was produced. The results of this experiment demonstrate that a strong cooperative effect can result if the etching surface is simultaneously exposed to a reactive gas and bombardment by energetic particles. The microscopic details of exactly how the ion bombardment enhances the reaction between a reactive gas and a surface, is the subject of substantial re-search efforts. Evidence indicates that different mechanisms exist for specific chemical systems.

Two principal mechanisms by which energetic ions assist in enhancing the etch rate produced by reactive gases, however, have been postulated to be operative in directional etching processes (Fig. 14-19).[21] They are the following:

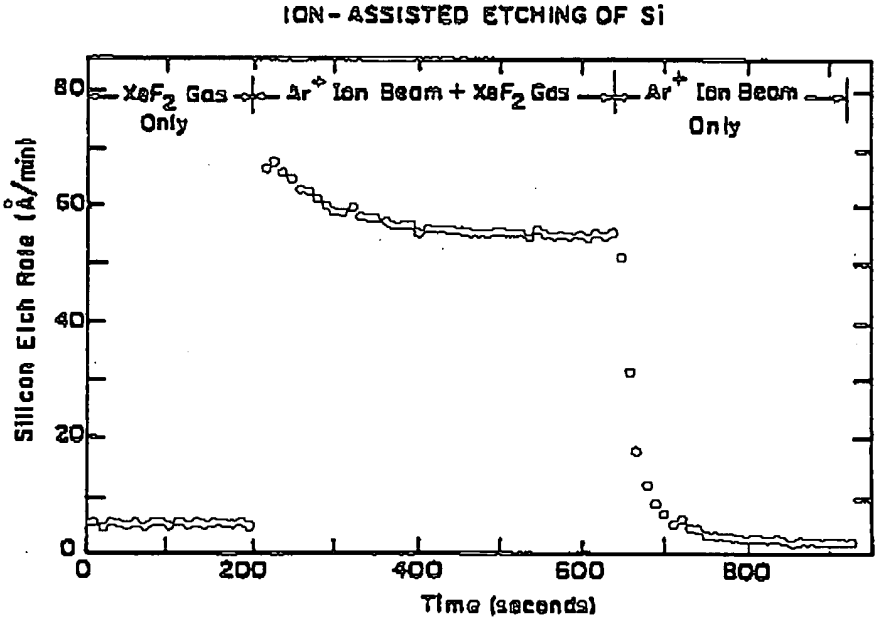

Fig. 14-18 An example of ion-assisted gas-surface chemistry in the etching of silicon with XeF_2. The XeF_2 flow is 2×10^{15} molecules/sec and the Ar energy and current are 450 eV and 2.5 μA, respectively.[26] Reprinted with permission of the American Physical Society.

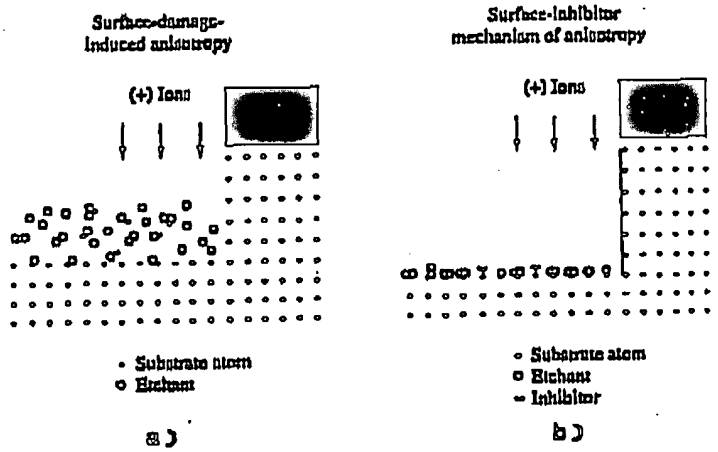

Fig. 14-19 (a) Surface damage, and (b) surface inhibitor mechanisms, for ion-assisted anisotropic etching.[21] Reprinted with permission of the American Physical Society.

1. Relatively high-energy impinging ions (>50 eV) produce lattice damage at the surface being etched, extending several monolayers beneath the surface. Reaction at these damaged sites is enhanced compared to reaction at surfaces at which no damage has occurred (i.e., the feature sidewalls that receive a much smaller flux of bombarding energetic ions).

2. Lower energy ions (≤50 eV) provide enough energy to desorb *nonvolatile polymer layers* (also referred to as *surface inhibiting*, or *blocking* layers) that deposit on the surfaces being etched. (These deposited polymer layers are only physisorbed on the surface, and require very little energy to desorb them.) In processes in which such polymer depositions occur, surfaces not struck by the ions retain their blocking layer, and hence are protected against etching by the reactive gas.

In features being etched on a wafer, the incident energetic particles generally arrive in a direction perpendicular to the wafer surface, and hence they strike the bottom surfaces of the etched features. The sidewalls of the etched features are subjected to little or no bombardment. As a result, the bottom of the features exhibit enhanced etching. Ion bombardment effects can be enhanced by decreasing the pressure in a high frequency (> 5 MHz) plasma, or by decreasing the frequency of the discharge.

Examples of specific data that illustrates anisotropic etching are given in the discussions on the etching of various film types, but two idealized examples are given here to illustrate the approaches that have been suggested to achieve directional etching. In the first case, shown in Fig. 14-20, hypothetical Si and SiO_2 surfaces are subjected to positive ion bombardment as a result of a negative bias voltage of -150 V being applied to the wafers.[17] Since the etch rate of SiO_2 is zero without ionic bombardment, but exhibits a finite rate under ion bombardment (Fig. 14-20), the SiO_2 film etches anisotropically. The Si etch rate is finite but smaller on surfaces that receive no ionic bombardment. Thus, the lateral etch rate is slower than the vertical etch rate. The etched feature ends up having a profile with non-vertical sidewalls.

In the second example, the chemistry of the discharge together with ionic bombardment is used to control the directionality of etching.[17] As was shown in the first hypothetical example, Si is etched more rapidly under energetic ion bombardment (e.g., from 150 eV ions) than when no bombardment occurs. If H_2 is added to the CF_4 feed gas, the Si etch rate decreases (Fig. 14-21). At some value of H_2 concentration, the non-bombarded-surface etch rate decreases to

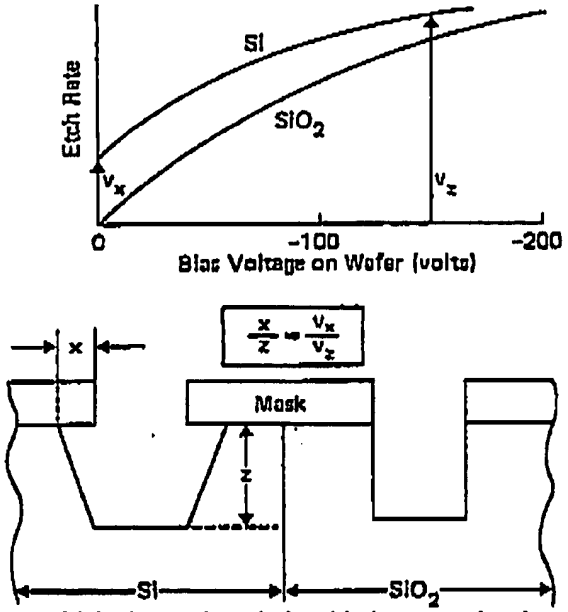

Fig. 14-20 Illustrative figure which shows the relationship between the shape of the etched wall profile and the dependence of the etch rate on the wafer potential.[17] Reprinted with permission of the American Physical Society.

zero, but the bombarded surfaces continue to be etched. Thus, under those conditions, the bottom of the feature is etched, while the non-bombarded sidewalls are not etched, and the resulting etched profile is vertical.

14.6 DRY-ETCHING VARIOUS TYPES OF MATERIALS IN ULSI APPLICATIONS

In the following sections details are provided about dry-etching processes used for various types of films used in IC fabrication.

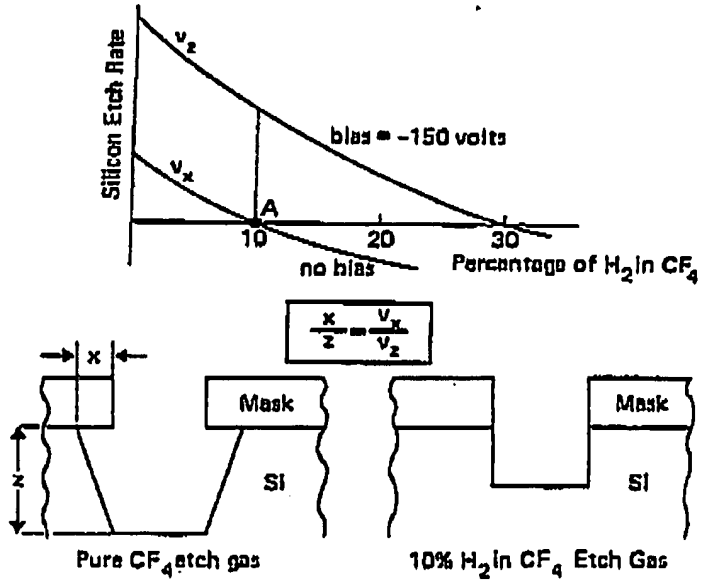

Fig. 14-21 Illustrative figure which shows the way in which the shape of a wall profile can be influenced by decreasing the fluorine-to-carbon ratio (in this example by H_2 addition).[17] Reprinted with permission of the American Physical Society.

14.6.1 Etching Silicon Dioxide (SiO_2)

Contact and via hole etching represent the most important applications involving SiO_2 etching in IC fabrication (although there are others, such as pad oxide and sacrificial oxide stripping, sidewall spacer etching in MOSFETs, etching of trenches for Damascene interconnect structures, and bond pad etching). The key issues of contact and via etching are the following: 1) sidewall profile control; 2) selectivity of the oxide etch process to the underlying silicon, polysilicon, or silicide; 3) selectivity of the oxide etch process to the photoresist; 4) etch rate uniformity of densely packed holes versus isolated holes (microloading); 5) etch rate uniformity of holes with different aspect ratios (ARDE, discussed in Sect. 14.6.1.3); and 6) etch residue removal from contact holes and vias. It was described earlier how fluorocarbon-containing plasma can be used to etch SiO_2, and how selectivity with respect to silicon can be obtained by using ion-bombardment and fluorine-deficient plasmas. Here the other issues are discussed. It should be noted that selectivity with respect to the silicon is an especially crucial issue for oxide etching. First, overetch is needed to clear all the contacts to the same level of silicon (e.g., the silicon substrate), and the Si in contacts that have been cleared are exposed to the oxide-etching plasma. Second, when etching contacts to both the polySi and the Si substrate in the same etch step, the oxide on top of the polysilicon layer is several hundred nanometers thinner than that over the silicon (Fig. 14-22).[27] In such bi-level etch processes, the exposed polySi must not be significantly etched as the remainder of the oxide thickness is etched down to the Si substrate. Oxide-to-silicon selectivities of greater than 25:1 are thus needed for 0.25 μm CMOS.

14.6.1.1 Shaping the Sidewalls of Contact Holes and Vias by Dry-Etching: When etching contact holes and vias in SiO_2, the desired profile of the contact hole sidewalls is dependent on the IC technology (i.e., the minimum feature size) and the type of interconnect structures being employed. Contact holes and vias with non-vertical sidewall profiles were used in IC generations down to about 0.35 μm CMOS. After that vertical sidewall profiles began to become necessary (since even slightly tapered contact holes and vias would encompass too much chip area, and this would represent an unacceptable functional density penalty).

For ICs from 2.0–0.8 μm that used 2 or 3 levels of metal (and in which Al is deposited into the contact holes and vias), the vias were made easier to fill by creating contact holes and vias with *wine-glass-shaped sidewalls* (see Fig. 16-17c) Such sidewall profiles are created using a two-step etch process. The top half of the intermetal dielectric film thickness is etched with an isotropic etch process, and the lower half with an anisotropic one. The isotropic process could

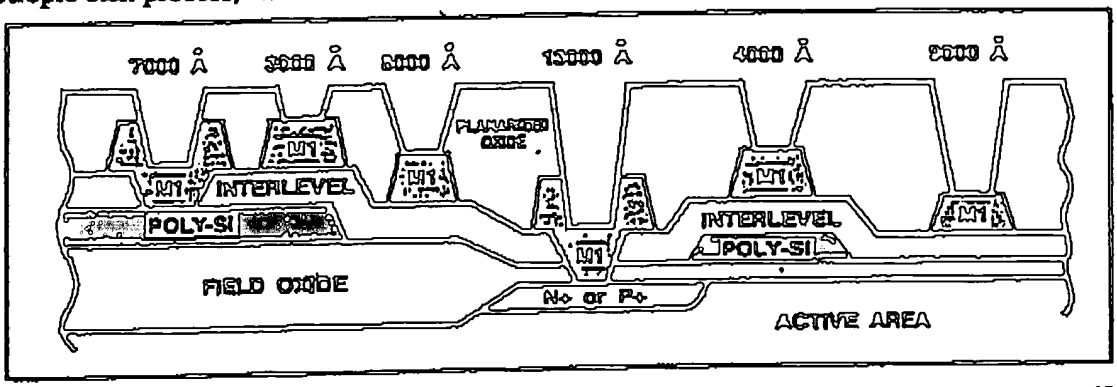

Fig. 14-22 Example which shows how much a via depth can vary in a double-level metal process if full planarization is achieved.[27] © IEEE (1986).

be either a wet-chemical-etch step or a dry-etch step. The isotropic dry-etch step would use a plasma that was fluorine rich and was created at medium pressure using a high-frequency rf power supply (13.56 MHz). That is, a $CHF_3 + O_2$, NF_3,[28] or SF_6 chemistry could be used for the isotropic dry-etch step. The lower half of the film would be etched using a fluorine-deficient plasma (e.g., CF_4/H_2, C_2F_6, or C_3F_8), operated at a low frequency (e.g., 450 kHz), and lower pressure. This would produce a CF_x deposition and energetic ion bombard-ment, conditions needed to create an anisotropic etch process with high selectivity to Si. Such a wine-glass-shape makes it easier to fill vias with Al, but it uses considerably more Si chip area than a vertical via with the same dimension as the bottom, anisotropically-etched portion of the via.

For ICs fabricated using 0.8–0.35 μm technologies, W-plugs were used to fill the contact holes and vias. These do not require a wine-shaped-glass via profile. That is, blanket CVD-W films can completely fill vias without voids or seams if the via profile is slightly sloped (i.e., ~85° slope). One method for producing such a slope is by a controlled polymer deposition on the contact hole sidewalls. Shown in Fig. 14-23 is a process where the polymer deposition rate on the sidewalls is high, and the etching proceeds in an anisotropic fashion (due to bombardment of the bottom of the hole being etched). Thus, as the contact hole is progressively being etched, the sidewalls at the top of the hole are being coated with a progressively thicker polymer. Since the etching at the bottom is anisotropic, this polymer buildup shadows the bottom of the hole, making its diameter progressively smaller. This results in a tapering of the contact hole sidewalls. Control of the rate of sidewall polymer deposition can be achieved by adjusting the chemistry of ratio of the polymerizing versus non-polymerizing constituents of the reactant gas feed[29] (e.g., by varying the ratio of CHF_3 and CF_4 gases in a CHF_3/CF_4 feedgas mixture). By increasing the percentage of CHF_3 in such a mixture, the polymer deposition rate (and hence angle of the sidewall taper) can be increased.[30] Other gases have also been used for this process, including mixtures of C_4F_8/N_2[31], $C_4F_8/Ar/CO/N_2/O_2$,[32] and $C_4F_8/CO/CHF_3$.[33] The process temperature also plays a role in the taper angle. Higher temperatures (e.g., ≥ 120°C) produce steeper sidewalls as the deposition rates of polymers are greater at lower temperatures. However, controllably producing tapered sidewalls on small SiO_2 contacts by an etching process remains a difficult task. The problem becomes more severe as aspect ratios increase. Eventually, non-tapered, straight-sided contact holes become the desired feature shape.

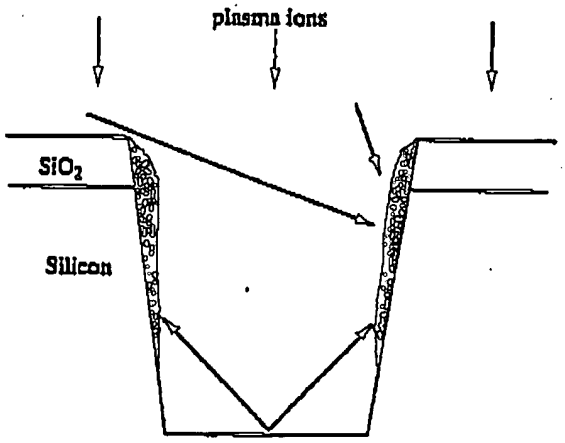

Fig. 14-23 The continuous buildup of sidewall polymer thickness in some dry etch processes results in a slope of the sidewalls of the contact hole being etched (if the etch process is anisotropic).